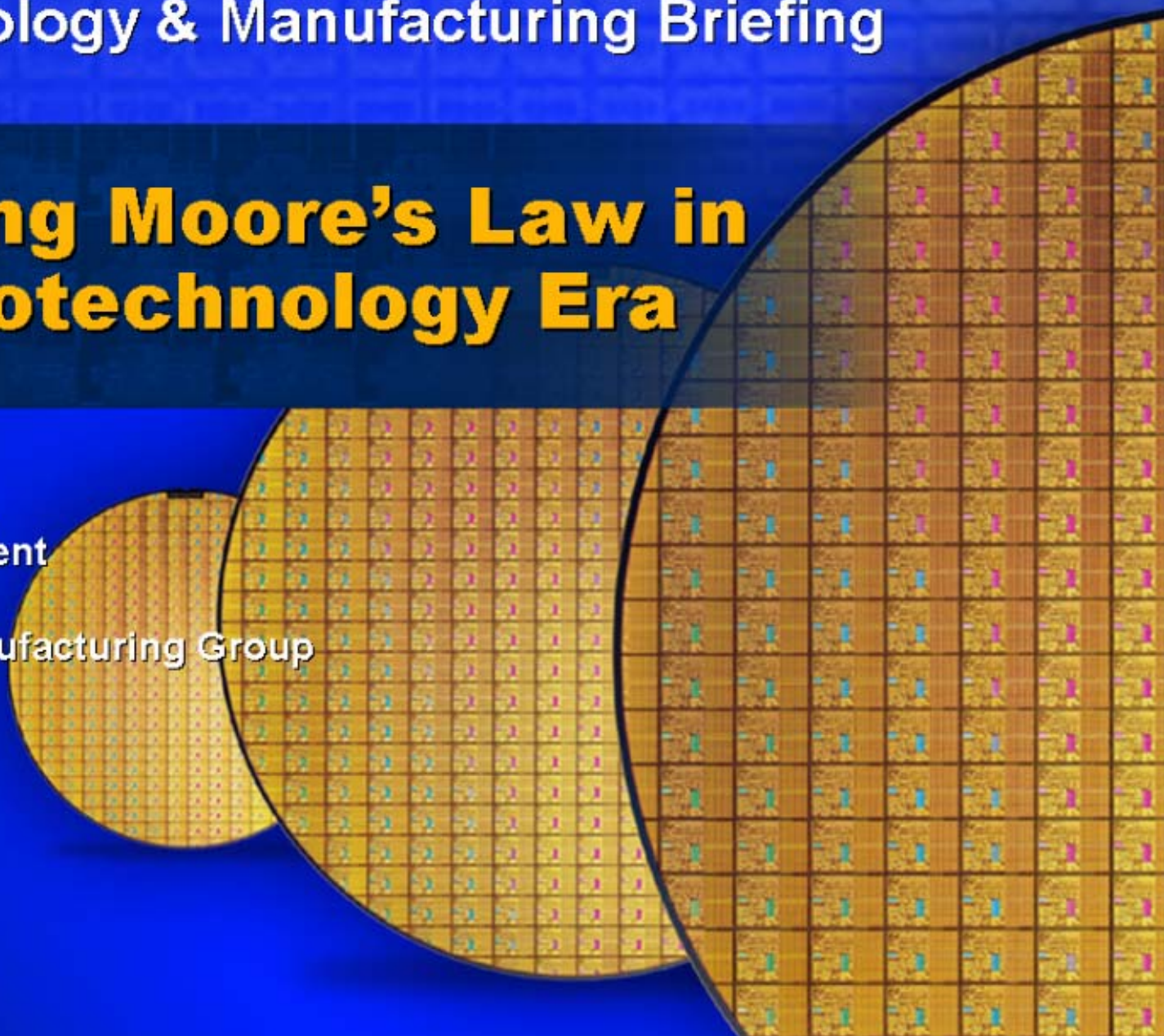
Intel Technology & Manufacturing Briefing

Extending Moore's Law in the Nanotechnology Era



Sunlin Chou
Senior Vice President
General Manager
Technology & Manufacturing Group

February 2004

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Key Points

- Intel will lead with 2-year technology cycles to extend Moore's Law for computing and communications
- Intel's 90nm technology is in volume production on 300mm wafers
- Innovations for 65nm and beyond are in Intel's R&D pipeline
- Nanotechnology will extend silicon technology into next decade

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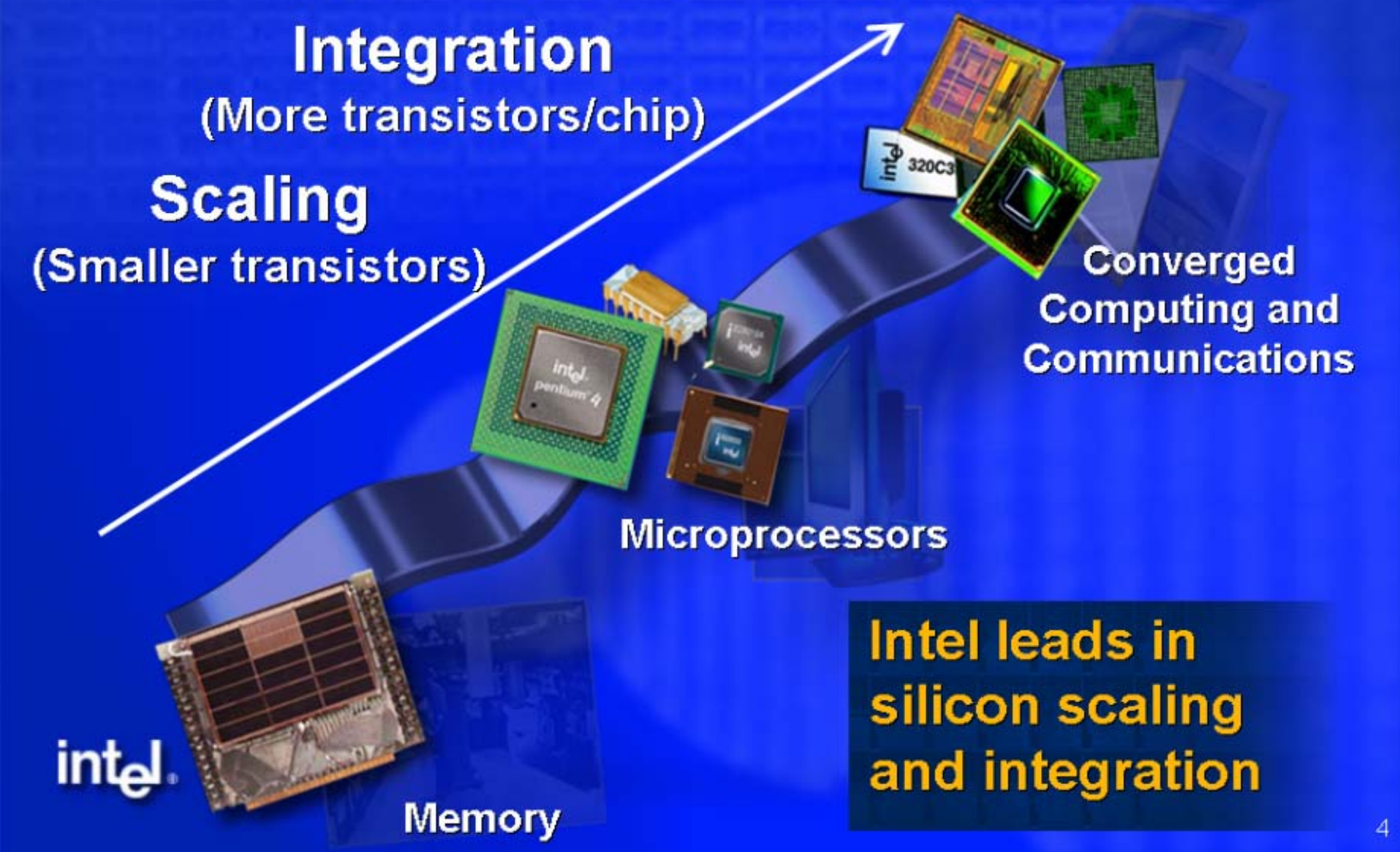
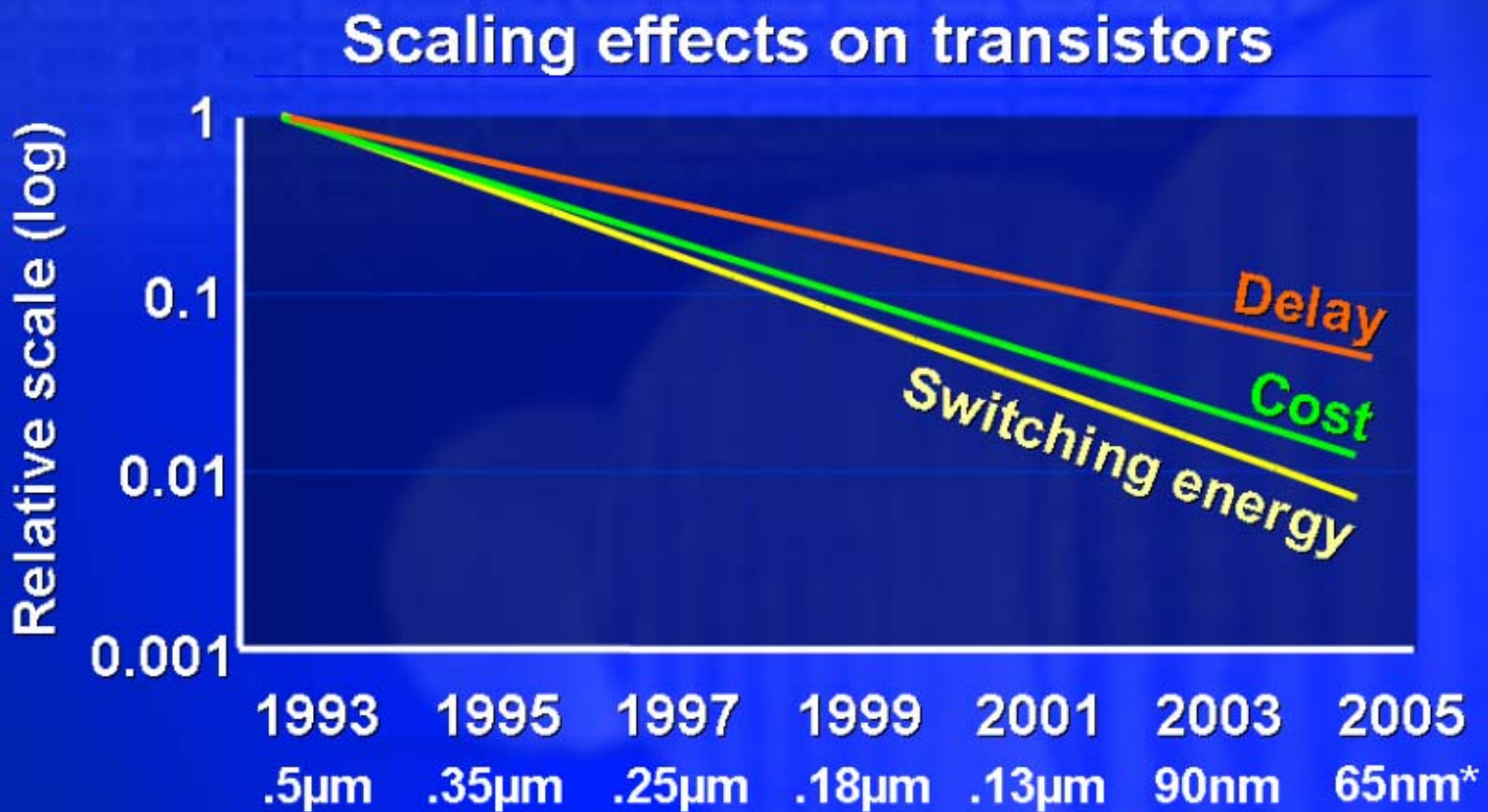
Computing + Communications Converge with Silicon Integration



Moore's Law Governs Performance, Power, Cost



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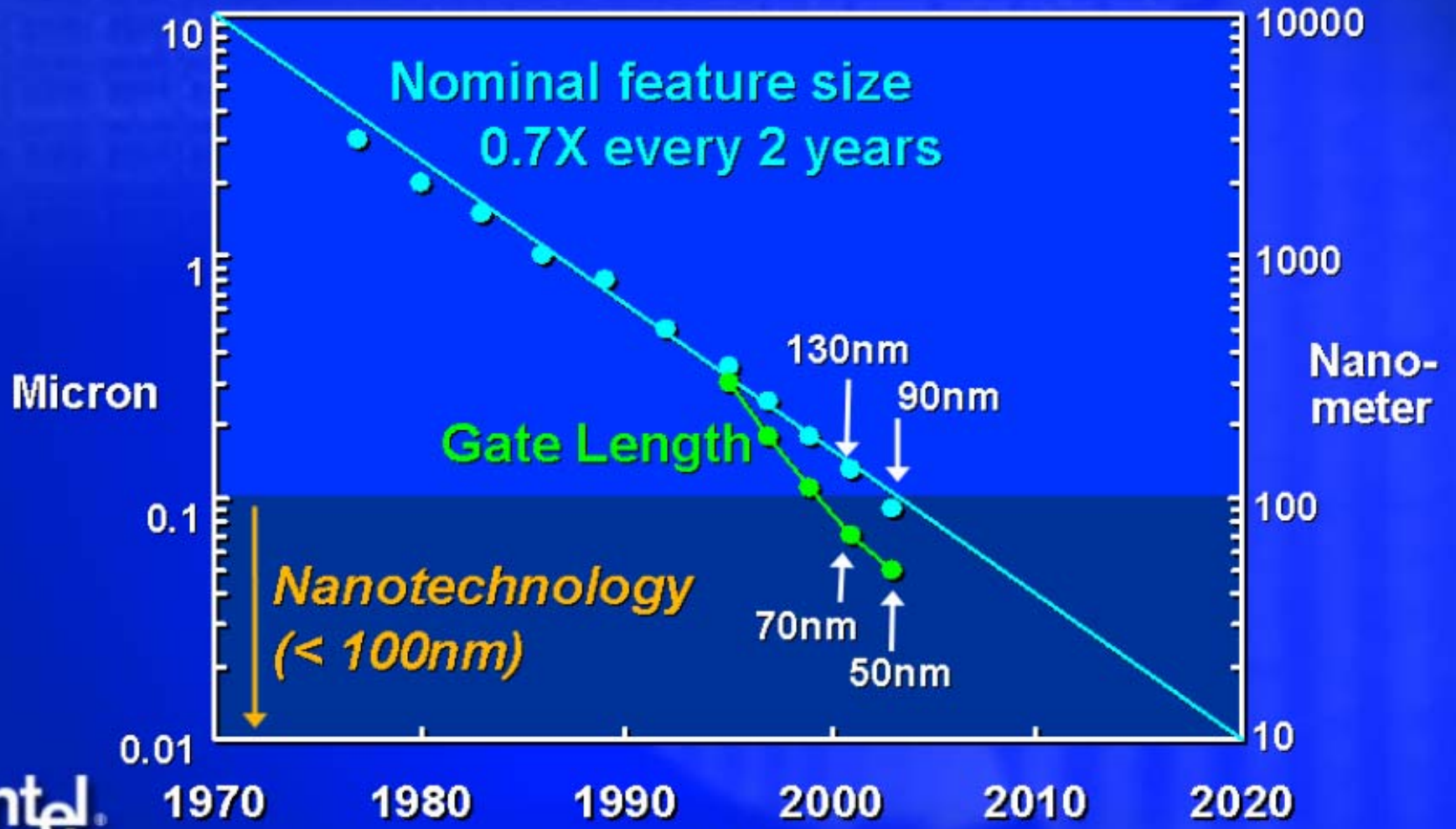
* Forecast

Source: Intel

Intel will Lead with 2-Year Cycles in Nanotechnology Era



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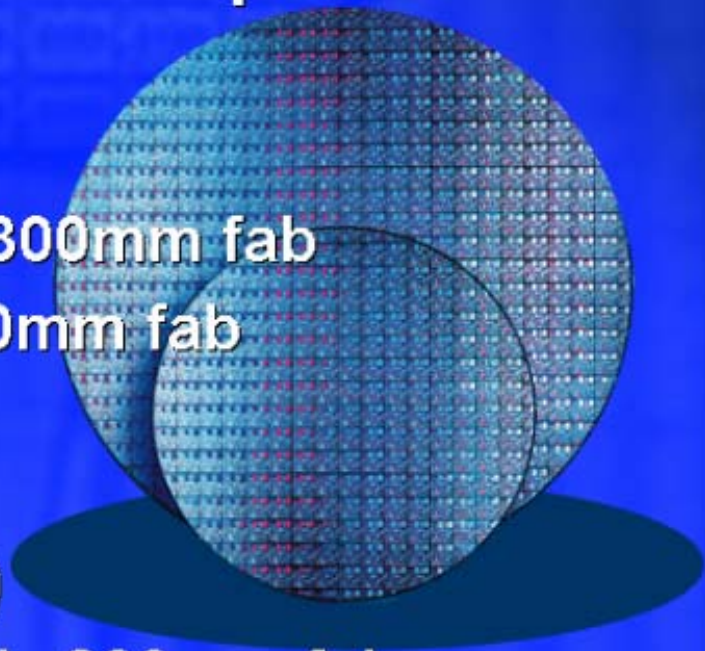
300mm Raises Value of Scale

- One 300mm fab produces more chips than two 200mm fabs
- Small scale producers
  - Insufficient volume to fill one 300mm fab
  - Stay with 200mm, or share 300mm fab
  - Economic benefits of 300mm unavailable/reduced
- Large scale producers (Intel)
  - Sufficient volume to fill multiple 300mm fabs
  - Grow internal capacity on 300mm
  - Gain economic, logistical benefits of 300mm



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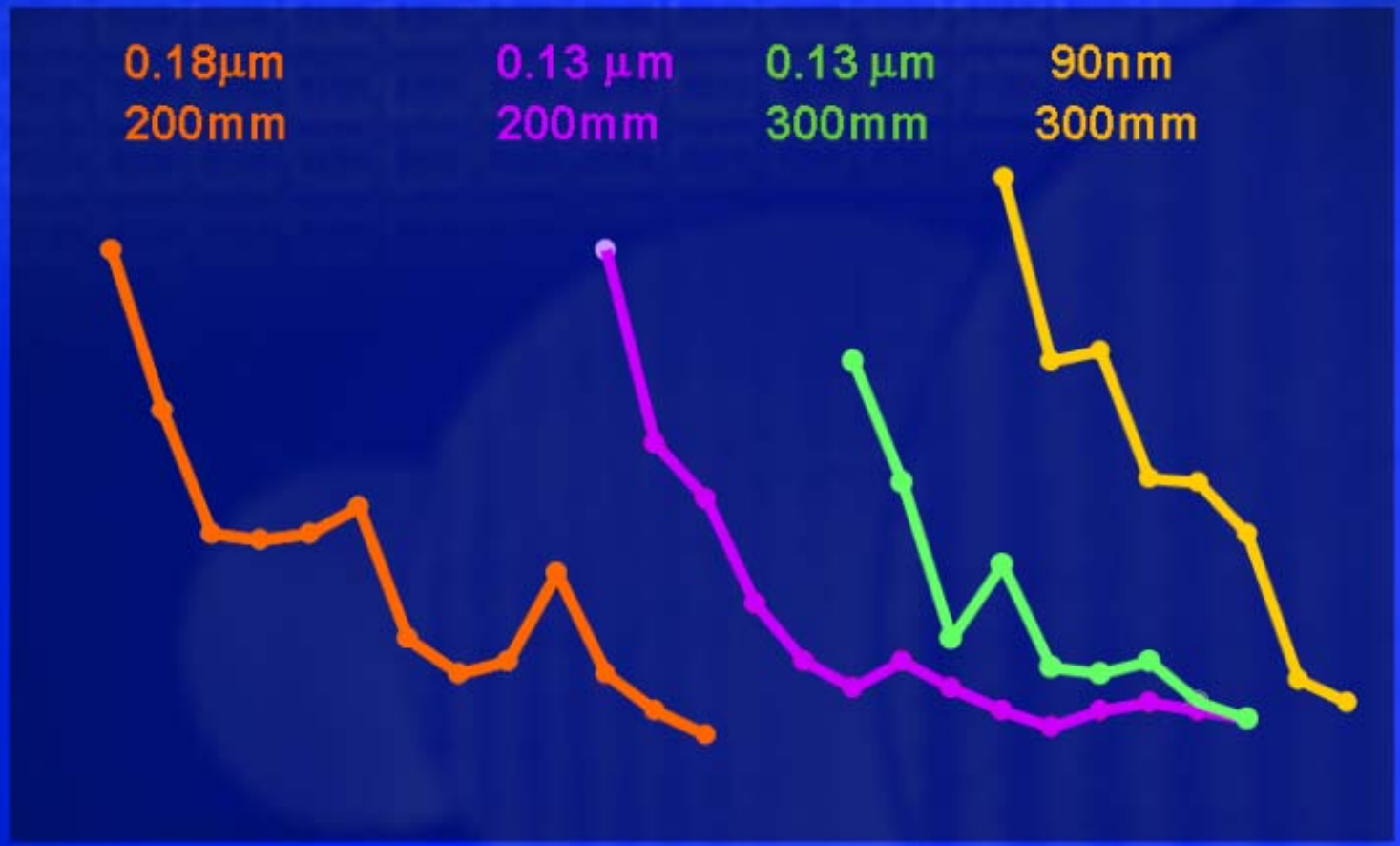
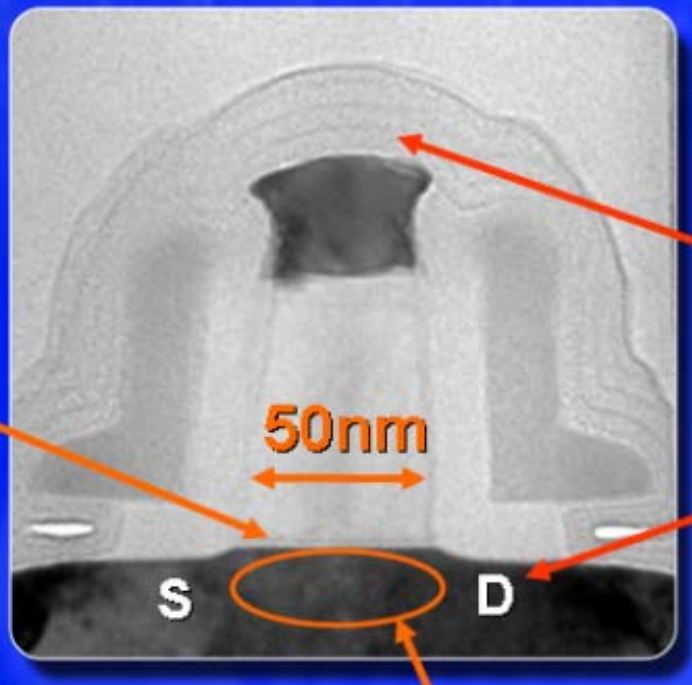
Intel's 90nm Process Yield Improved at Record Rate



Source: Intel

Intel's Transistors Run Fast on 90nm Strained Silicon Process



1.2nm Gate Oxide

Strain Inducers

Silicon Nitride Cap (NMOS)

SiGe Source-Drain (PMOS)

Strained Silicon Lattice

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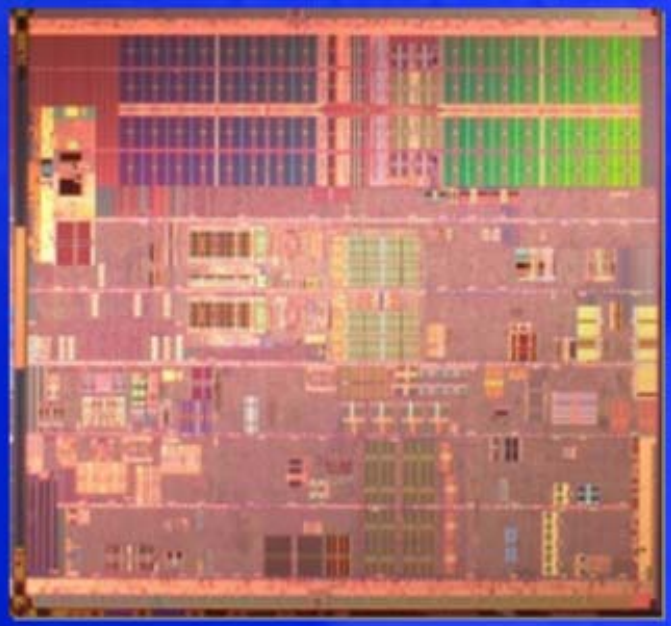
Source: Intel

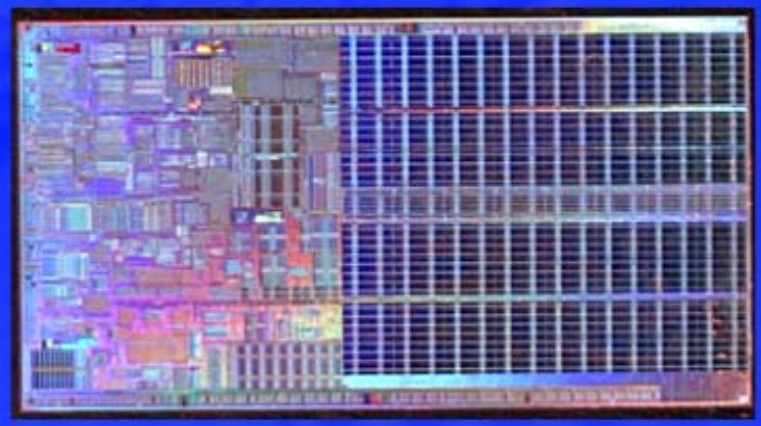
Intel's 90nm Processor Chips

Prescott CPU



112 mm^2 die size
125 million transistors
1M cache

Dothan CPU



87 mm^2 die size
140 million transistors
2M cache

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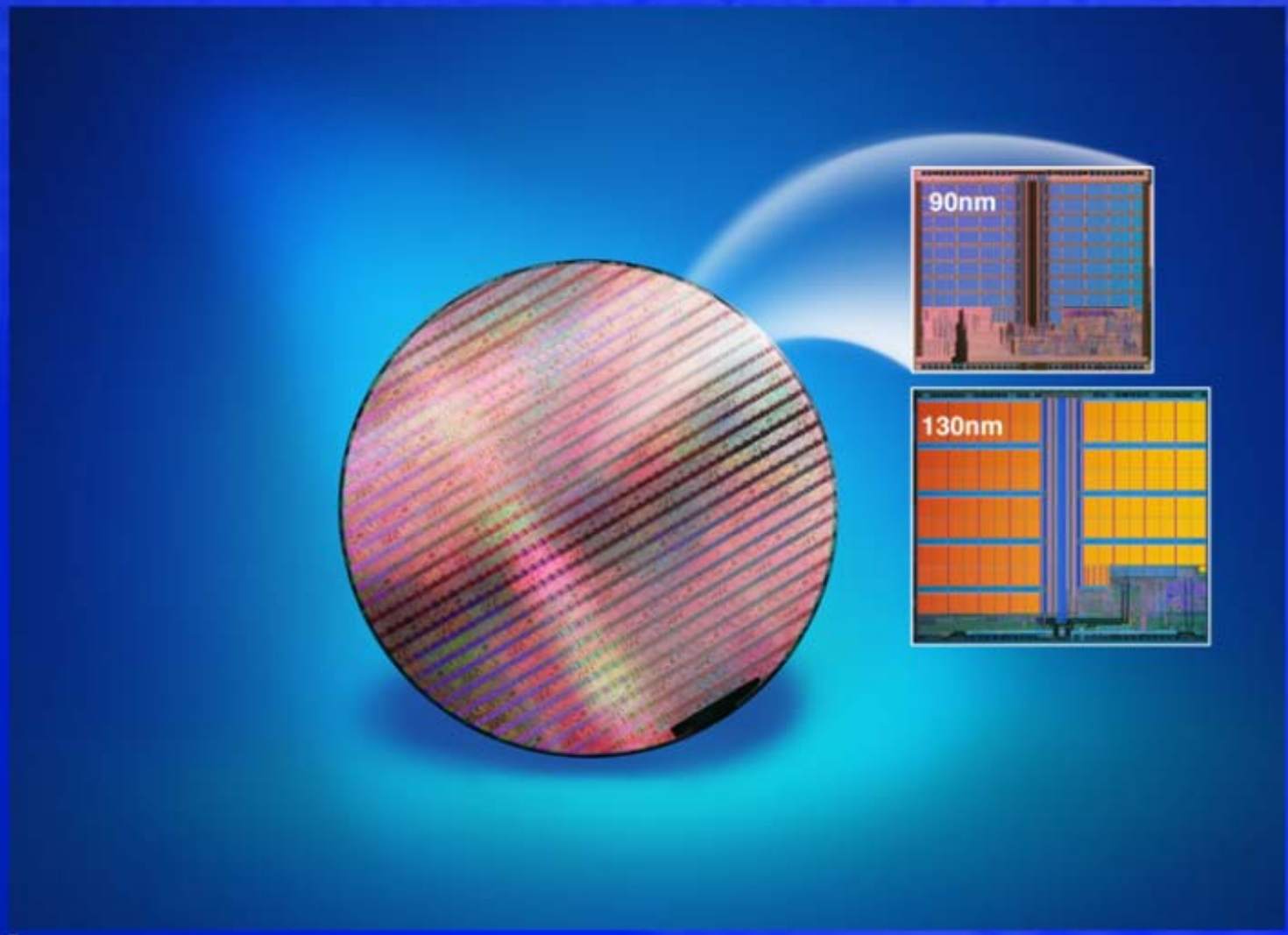
On-chip cache content increasing

Source: Intel

Intel's 90nm NOR Flash Memory



200 mm wafer

Source: Intel

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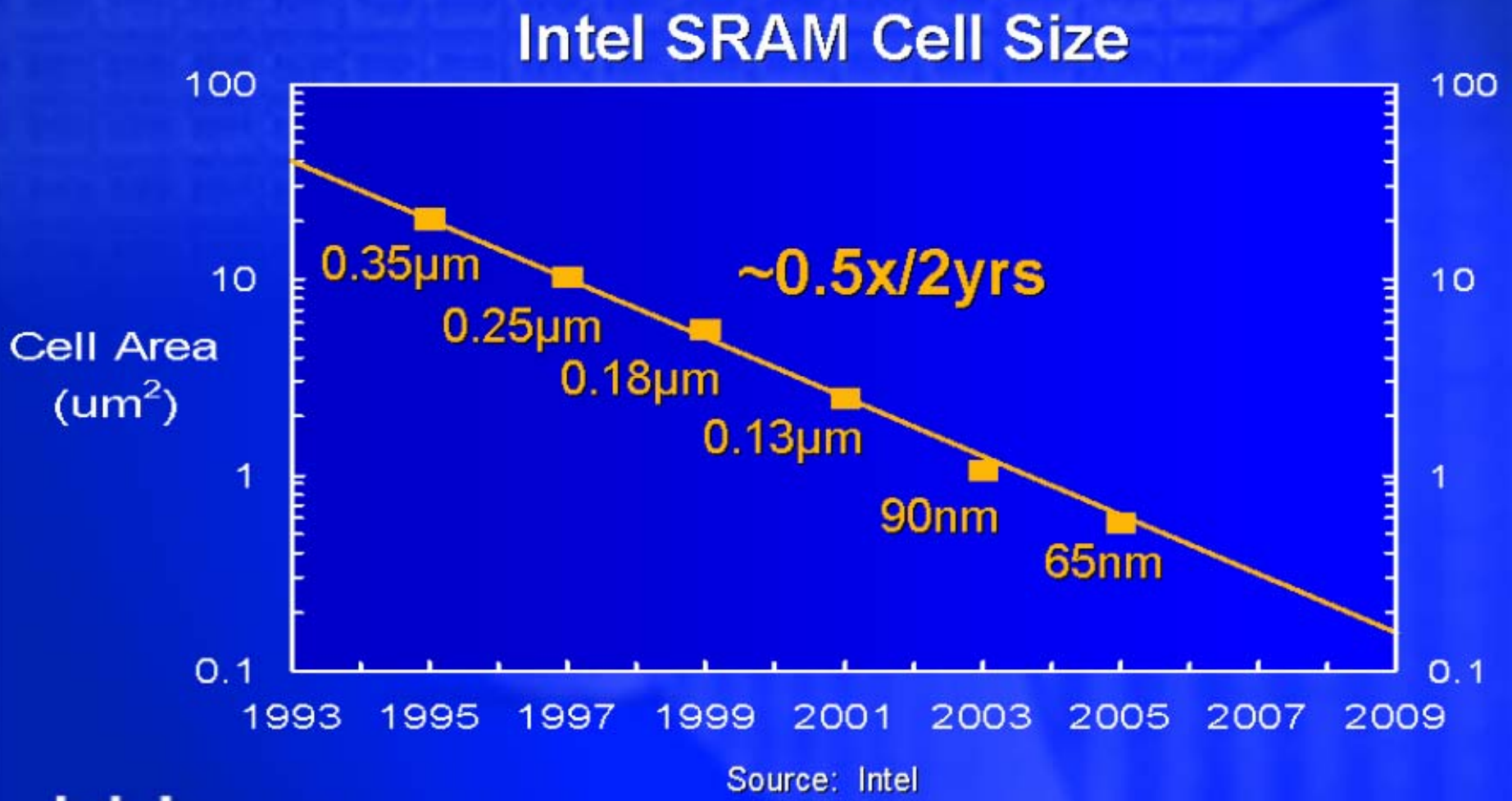
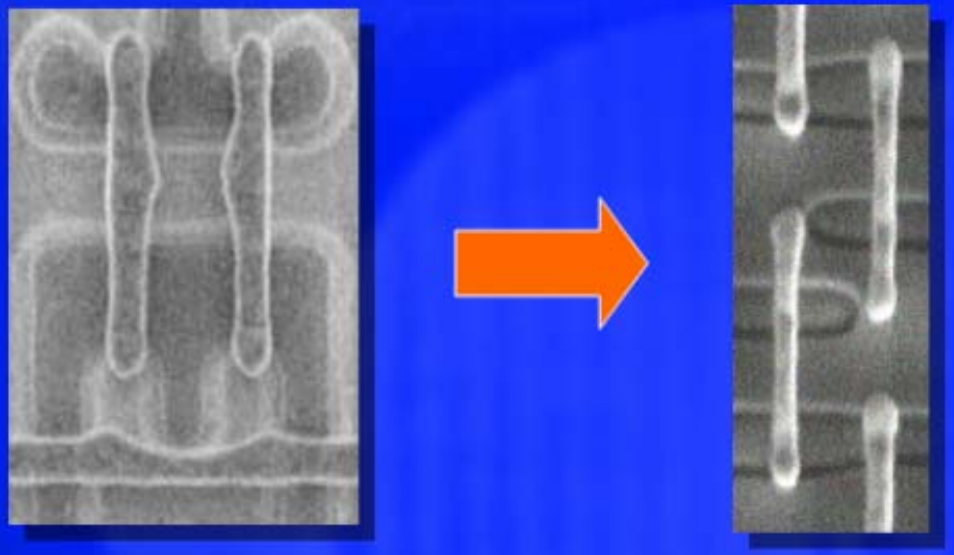
Cell Size Reduction Continues on 2-Year Pace



SRAM Cell Size Reduced on 65nm Process

90nm Process (3/2002)

65nm Process (11/2003)



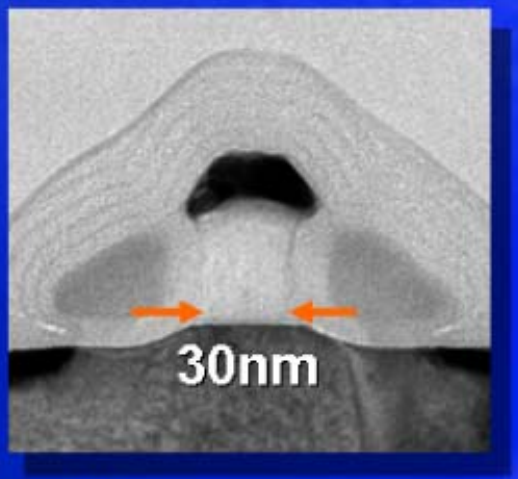
$1\mu m^2$ SRAM Cell

$0.57\mu m^2$ SRAM Cell

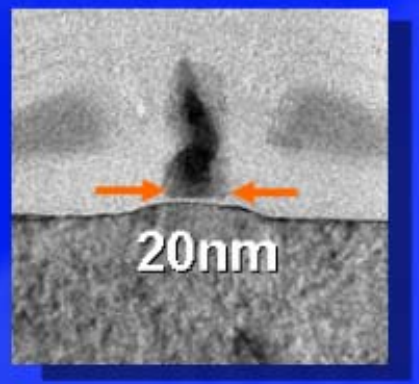
Source: Intel

Intel's Transistor Research in Deep Nanotechnology Space

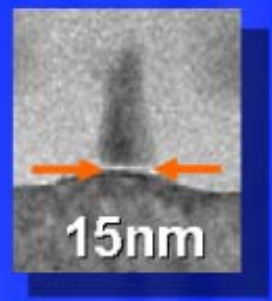
Experimental transistors for future process generations



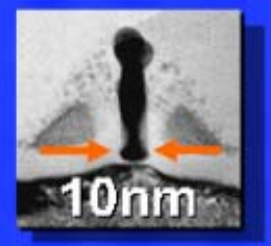
65nm process
2005 production



45nm process
2007 production



32nm process
2009 production

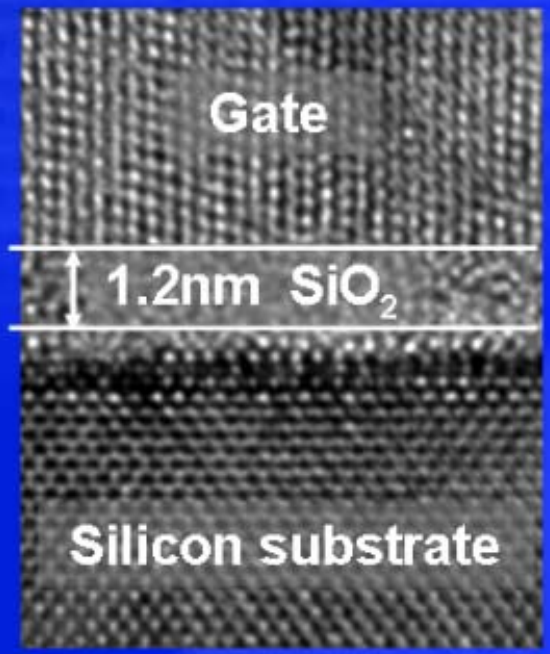


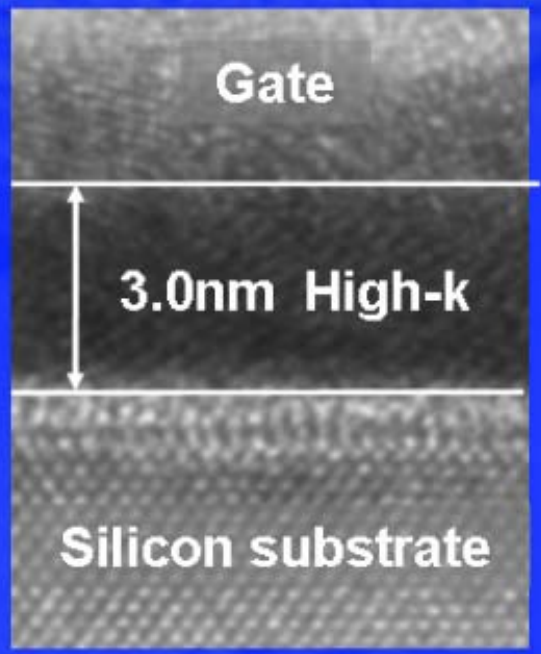
22nm process
2011 production

intel Transistors will be improved for production

Source: Intel forecast

High-k Dielectric Reduces Leakage





	High-k vs. SiO_2	Benefit
Gate capacitance	60% greater	Faster transistors
Gate dielectric leakage	> 100x reduction	Lower power

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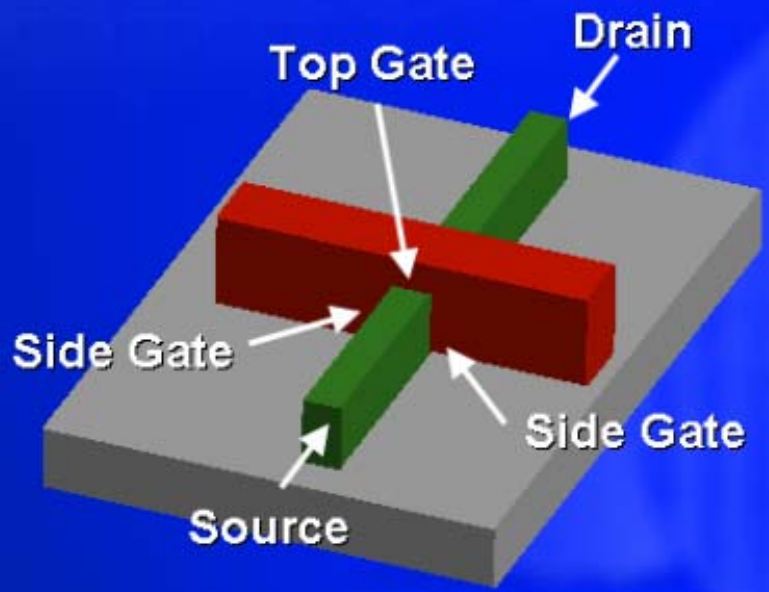
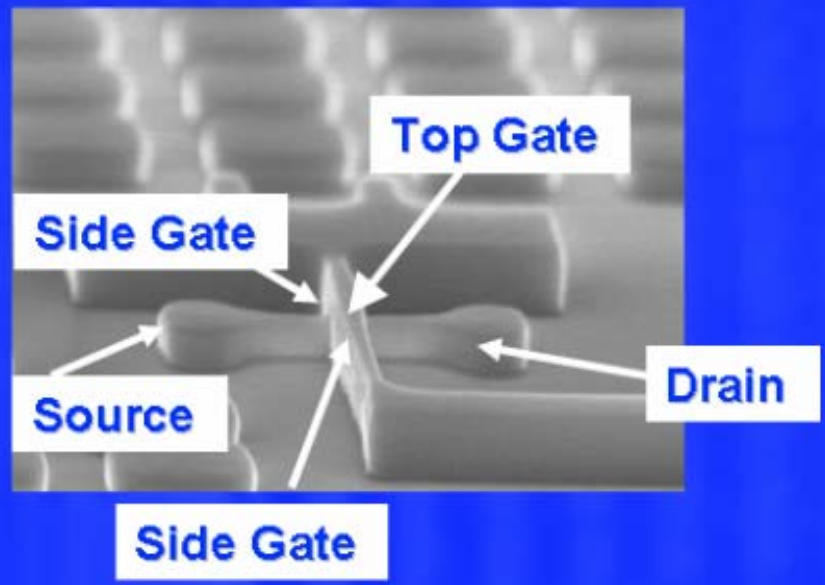
Transistors Improved by Going 3-D

Intel's experimental Tri-gate transistor raises performance, lowers off current





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Source: Intel

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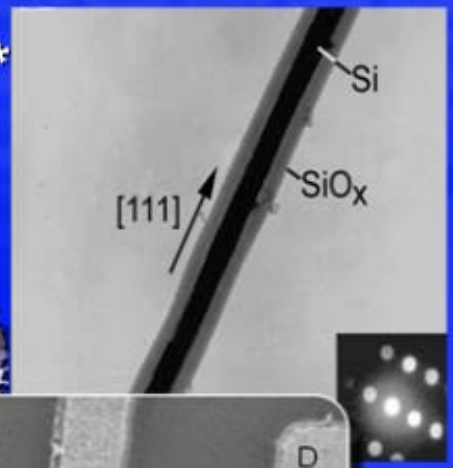
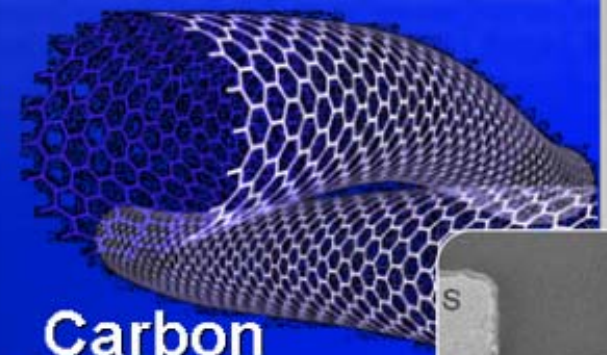
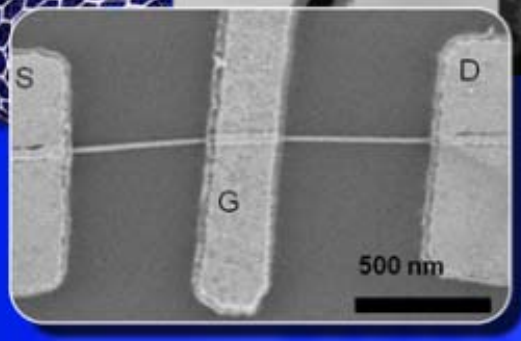
Future Nanotechnology will Ride on Silicon Technology Base

Silicon Nanowire*



Carbon Nanotube





Nanotube/Nanowire Transistors

Molecular Electronics Nanodevices

intel Innovations will extend silicon technology

*Source: Morales & Lieber, Harvard Univ

Nanotechnology Brings Welcomed Opportunities

- Renewal and extension of silicon technology
  - New materials, processes and device structures
  - Integrate innovations into silicon technology base
  - Extend device scaling and Moore's Law
- Intel plans to lead in nanotechnology
  - Already in production with nanotechnology
  - Heavily engaged in nanotechnology R&D
  - Best positioned to use nanotechnology innovations

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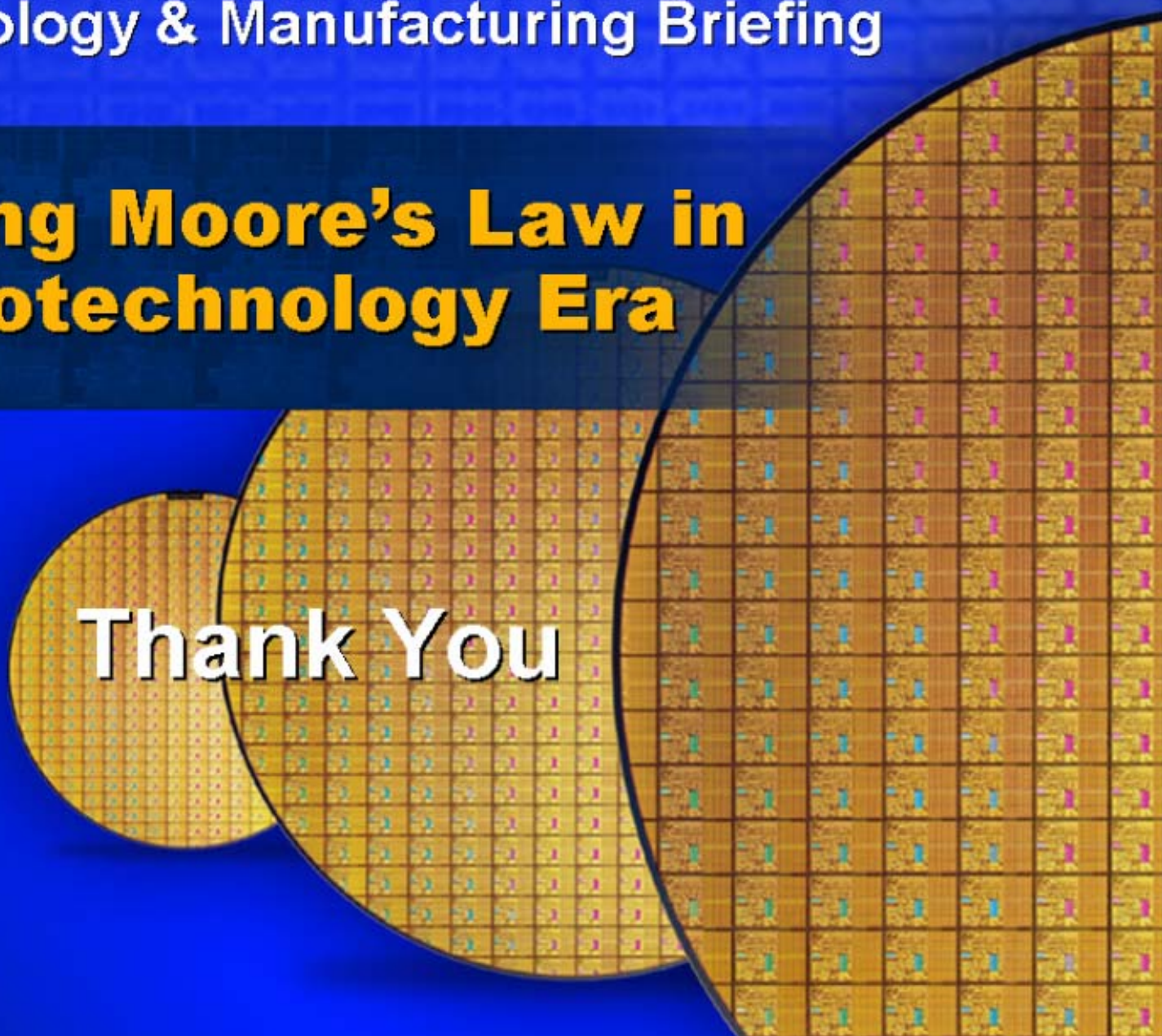

Thank You

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Risk Factors

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